material only substantially under each conductive pattern of the conduct layer formed thereon and each dielectric layer comprises a second dielectric material between and adjoi each portion of the first dielectric material, and the second dielectric material of each dielectric layer has dielectric constant less than the dielectric constant of the first dielectric material and comprises a polyimide or other organic dielectric, wherein the first dielectric material is silicon dioxide.

2. A semiconductor device comprising a plurality of sequentially formed dielectric and conductive layers, each conductive layer comprising at least one conductive pattern; wherein each dielectric layer comprises a portion consisting essentially of a first dielectric material only substantially under each conductive pattern of the conductive layer formed thereon and further comprising a thin conformal dielectric coating thereon and a topside dielectric layer formed on the thin conformal dielectric coating, wherein the topside dielectric layer comprises a dielectric material having a dielectric constant less than the dielectric constant of the conformal dielectric coating and the topside dielectric layer comprises a polyimide or other organic dielectric, wherein the first dielectric material is silicon dioxide.

3. The semiconductor device according to claim 2, wherein the conformal dielectric coating comprises a silicon oxide, silicon nitride or a silicon oxynitride.

4. A semiconductor device comprising a plurality of sequentially formed dielectric and conductive layers, each conductive layer comprising at least one conductive pattern; wherein each dielectric layer comprises a portion of a first dielectric material only substantially under each conductive pattern of the conductive layer formed thereon and further comprising a first thin conformal dielectric coating and a second thin conformal dielectric coating formed thereon, wherein the dielectric constant of the first conformal dielectric coating is greater than the dielectric constant of the second conformal dielectric coating, wherein the second conformal dielectric layer comprises a polyimide or other organic dielectric and the first conformal dielectric coating comprises a silicon oxide, silicon nitride or a silicon oxynitride.

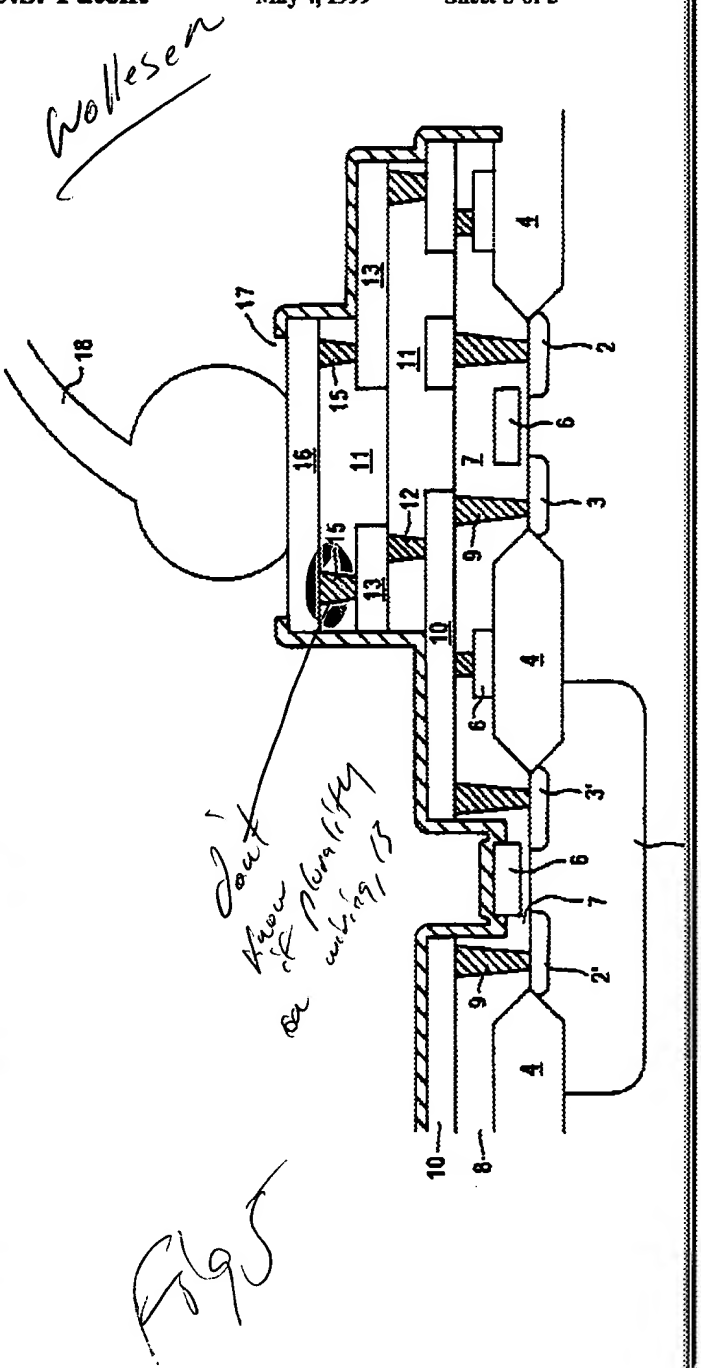

Fig 5

circuitry, by significantly reducing the capacitance of the interconnection pattern. Basically, the present invention commences where conventional practices terminate. Specifically, the present invention begins with a conventionally formed semiconductor device as depicted in FIG. 1, prior to integrating the FIG. 1 device into a circuit. Thus, the practice of the present invention initially involves conventional manufacturing procedures to produce the semiconductor device schematically depicted in FIG. 1.

(3) The present invention comprises selectively removing the sections of dielectric material from each dielectric layer, initially formed of a first dielectric material, leaving a portion of the first dielectric material only substantially under each conductive pattern of the conductive layer formed on the dielectric layer for structural support. This simplified, cost effective technique can be accomplished by employing anisotropic etching, such as a conventional plasma etch, to remove sections of the dielectric layers which are not substantially under conductive patterns. Typically, dielectric layers are formed of oxides and nitrides, such as silicon oxide and silicon nitride. In accordance with the present invention, anisotropic etching can be timed or determined using a conventional end point detection technique at a conductive layer. In conducting anisotropic etching, it is preferred to anisotropically etch all dielectric layers in one etching stage to increase processing throughput.

(4) The anisotropic etching techniques employed in practicing the present invention, do not remove significant amounts of conductive material, typically conductive employed in interconnection patterns. Such typical conductive materials include aluminum, polysilicon and refractory metals. The present invention, however, is not limited to any particular dielectric materials as the first dielectric material, or to any particular conductive material, but includes copper, copper-based alloys, gold, gold-based alloys, silver, silver-based alloys, aluminum, aluminum-based alloys, refractory metals, refractory metal alloys, refractory metal compounds and superconducting materials.

(5) Thus, in accordance with the present invention, sections of the first dielectric material are removed from the dielectric levels of a multilevel semiconductor device, thereby leaving air

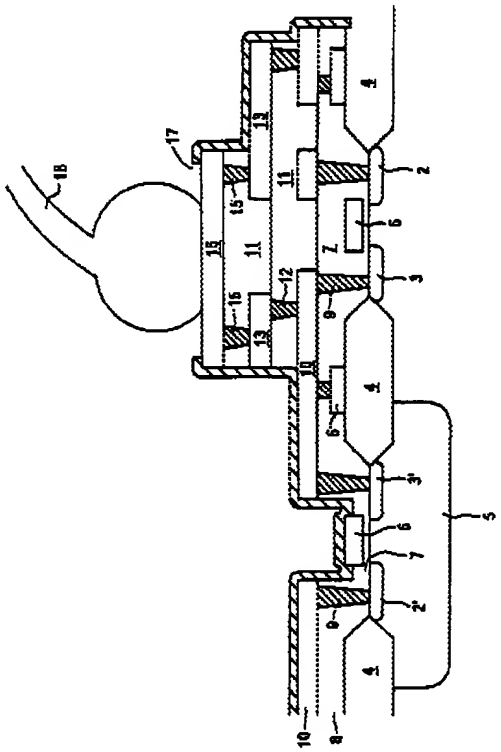

Figure 5

Cu, L56-67

then be removed to enable external connection.

Detailed Description Text - DETX (14):
FIG. 5 shows the implementation of a package interconnection. Elements in FIG. 5 similar to those in FIGS. 1, 2, 3 and 4 bear similar reference numerals. Bond pad opening 17 is added, as to the FIG. 3 embodiment, to indicate the connection of the metal layer (typically aluminum) to the package interconnect means. As shown in FIG. 5, a thermo-compression "ball bond" 18 is provided for electrical contact to the product die. Whereas the interconnect capacitance is reduced by removing dielectric material between the interconnect, dielectric material underneath the metal interconnect layer is not removed. This is an advantage, because wire bonding results in the application of large mechanical forces to the bond pad metal during packaging manufacture. It also allows the addition of "bumps" on the die for subsequent "flip chip" assembly or TAB bonding (Tape Automated Bonding). Because the standard metal and dielectric materials remain underneath the bond pad metal on the die, the mechanical support enjoyed by prior art (FIG. 1) is retained, allowing standard manufacturing practices for package assembly to be employed in practicing the present invention without any change. Approaches involving the use of an air bridge require the addition of special mechanical structures, thereby introducing process complexity in order to use standard wire bonding techniques, or requiring modification of standard package manufacturing practices. The assembly bonding advantage of the present invention applies to all embodiments.

Detailed Description Text - DETX (21):
The various embodiments of the present invention may comprise the use of damascene techniques, such as single and dual damascene techniques. In dual damascene techniques, vias and trenches are simultaneously filled with conductive material conventionally employed in fabricating interconnection structures, preferably with the use of a barrier layer.

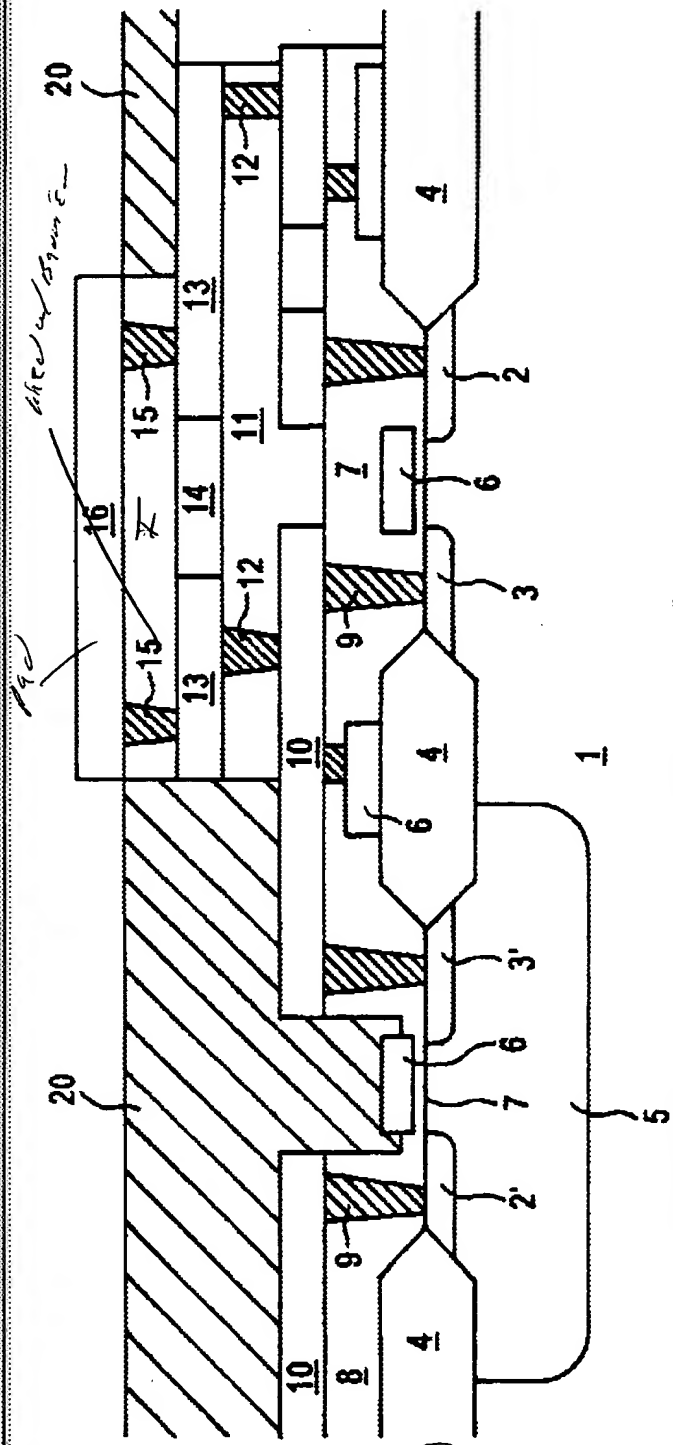

Figure 2

DOCUMENT-IDENTIFIER: US 20020005582 A1

TITLE: Pad structure for copper interconnection and its formation

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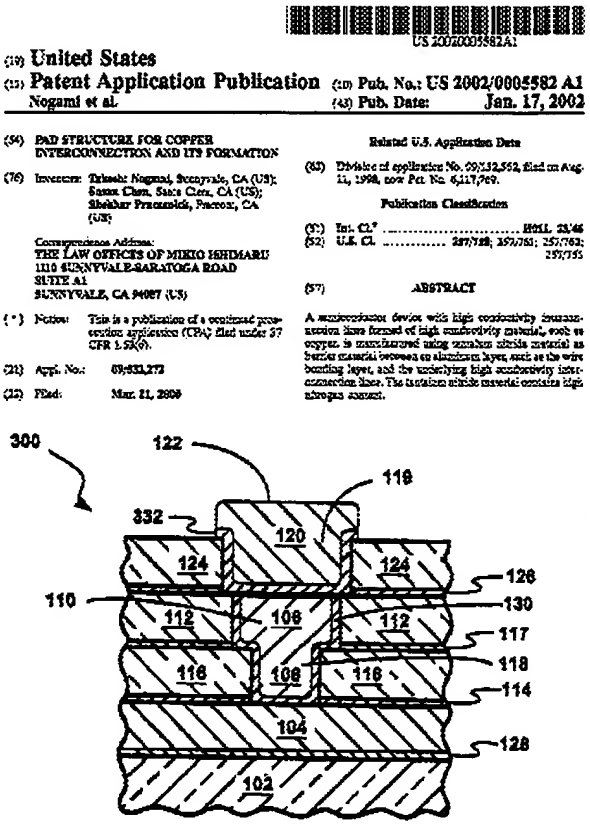
Abstract Paragraph - ABTX (1):
A semiconductor device with high conductivity interconnection lines formed of high conductivity material, such as copper, is manufactured using tantalum nitride material as barrier material between an aluminum layer, such as the wire bonding layer, and the underlying high conductivity interconnection lines. The tantalum nitride material contains high nitrogen content.

Title - TTL (1):
Pad structure for copper interconnection and its formation

Summary of Invention Paragraph - BSTX (2):
[0002] The present invention relates generally to semiconductors and more specifically to barrier materials and pad structures used in semiconductor devices comprising high conductivity interconnection lines.

Summary of Invention Paragraph - BSTX (4):
[0003] Conventional semiconductor devices typically are made up of a semiconductor substrate, normally a monocrystalline silicon with a plurality of dielectric and conductive layers formed thereon. An integrated circuit is formed of semiconductor devices connected by a plurality of spaced-apart conductive lines and a plurality of interconnection lines, such as bus lines, word lines and logic interconnection lines. Such interconnection lines generally constitute a limiting factor in terms of various functional characteristics of the integrated circuit. There exists a need to provide a reliable interconnection structure capable of achieving higher operating speeds, improved signal-to-noise ratio, improved wear characteristics, and improved reliability.

Summary of Invention Paragraph - BSTX (8):
[0007] According to conventional practices, a plurality of conductive layers are formed over a semiconductor substrate, and the uppermost conductive layer joined to a bonding pad for forming an



US 20020005582A1

(19) United States
(12) Patent Application Publication (10) Pub. No.: US 2002/0005582 A1
Nogami et al. (43) Pub. Date: Jan. 17, 2002

(54) PAD STRUCTURE FOR COPPER INTERCONNECTION AND ITS FORMATION

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(21) Appl. No.: 09/833,272

(22) Filed: Mar. 21, 2000

Related U.S. Application Data

(62) Division of application No. 09/132,552, filed on Aug. 11, 1998, now Pat. No. 6,117,769.

Publication Classification

(51) Int. Cl.[7] H01L 23/48

(52) U.S. Cl. 257/758; 257/751; 257/762; 257/755

(57) ABSTRACT

A semiconductor device with high conductivity interconnection lines formed of high conductivity material, such as copper, is manufactured using tantalum nitride material as barrier material between an aluminum layer, such as the wire bonding layer, and the underlying high conductivity interconnection lines. The tantalum nitride material contains high nitrogen content.

onto the barrier metal layer 18. The interconnection layer 19 extends over the bonding pad region 9 and the diffusion regions 2, 3 and defines a binding pad 30 over the openings 7 and the conductive layer 15. A protective insulation layer 20 covers the interconnection layer 19. A pad opening 23 is provided in the insulation layer 20 to expose the interconnection layer 19 in the bonding pad region 9.

(12) Thus, the barrier metal layer 18 is fixed through openings in the insulation insulator 14, to a conductive layer 15, and the interconnection layer is formed on the barrier metal layer. Accordingly, the barrier metal layer and the interconnection layer are firmly secured or anchored onto the region of the bonding pad.

(13) A process for fabricating the above semiconductor device is now described with reference to FIGS. 2(a)-2(e).

(14) FIG. 2(a) shows a cross section of a stage of fabrication of the semiconductor device according to the preferred embodiment of the invention. More specifically, at this stage, the diffusion regions 2, 3, are doped by ion implantation to have a conductivity type opposite to that of the substrate 1, and to retain lightly doped regions 4, 5, which form a part of the LDD structure. To isolate the active regions from each other, the thick, field oxide, isolation layer 6 is formed on the substrate 1, as by a selective oxidation process well known to those skilled in the semiconductor art.

(15) The gate electrode 11, over the thin gate oxide 10, comprises a layer of polysilicon, silicide, refractory metal, polycide, or the like. When the gate electrode is formed, the conductive layer 15 is simultaneously formed using the same gate material. The oxide side walls 12, 13 and 16, 17 are formed on the opposite sides, respectively, of the gate electrode 11 and the conductive layer 15. The side walls 12, 13 serve to mask the lightly doped regions 4, 5 during the high density doping of the diffusion regions 2, 3.

(16) As shown in FIG. 2(b), after the doping of the diffusion regions 2, 3, the oxide interlayer insulator (insulation layer) 14, which may contain phosphorus or boron as an impurity, is deposited over the entire surface of the substrate 1, using a CVD process. As a result, the gate electrode 11 and the conductive layer 15 are covered with the

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US005357136A

United States Patent [19]
Yoshioka

[11] Patent Number: 5,357,136
[45] Date of Patent: Oct. 18, 1994

[54] SEMICONDUCTOR DEVICE WITH ANCHORED INTERCONNECTION LAYER

[75] Inventor: Kentaro Yoshioka, Chiramura, Japan

[73] Assignee: Oki Electric Industry Co., Ltd., Tokyo, Japan

[21] Appl. No.: 42,401

[22] Filed: Apr. 2, 1993

[30] Foreign Application Priority Data

Apr. 10, 1992 [JP] Japan 4-090719

[51] Int. Cl.5 .... H01L 27/02; H01L 23/48; H01L 29/46

[52] U.S. Cl. 257/383; 257/384; 257/385; 257/755; 257/751; 257/753; 257/757; 257/764

[58] Field of Search 257/382, 383, 384, 385, 257/739, 751, 753, 757, 764

[56] References Cited

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FOREIGN PATENT DOCUMENTS

2-16719 1/1990 Japan 257/384

Primary Examiner—Ngan Van Ngo
Attorney, Agent, or Firm—Steven M. Rabin

[57] ABSTRACT

A semiconductor device having a bonding pad region, and a method of its fabrication. A conductive layer is formed on an isolation layer separating transistors of the device, to anchor the interconnection layer on the bonding region. The conductive layer may be formed from the same layer of material that gate electrodes of the transistors are formed. An oxide insulation layer covers the conductive layer and has at least one opening exposing the conductive layer in the bonding pad region. A barrier metal layer, formed on the diffusion regions and the insulation layer, extends into the opening where it makes a firm direct connection with the exposed conductive layer. A bonding pad is formed on the barrier metal layer by providing the interconnection layer on the barrier metal layer. Since the conductive layer and the barrier metal layer are firmly connected, and secures the interconnection layer in the bonding pad structure. According to a method of fabrication, the conductive layer is formed on the isolation layer simultaneously with the formation of the gate electrode, and then covered by the insulation layer. The openings are then provided in the insulation layer to expose the conductive layer. The barrier metal layer is then formed on the insulation layer so that it contacts the diffusion region and extends into the opening to become fixed to the conductive layer. The interconnection layer is then formed on the conductive layer.

19 Claims, 4 Drawing Sheets

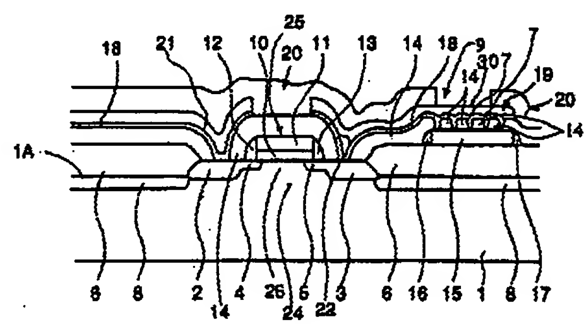

Fig. 2e

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(4) 1. Field of the Invention

(5) This invention relates to a semiconductor device and, more particularly, to a MOS (Metal-Oxide-Silicon) integrated circuit device having an improved bonding pad structure.

(6) 2. Description of Related Art

(7) The use of barrier metal technology is inevitable for 0.5 micron designs of semiconductor devices. In a process of fabricating a semiconductor device containing MOS transistors, to which the barrier metal technology is applied, a thick field oxide layer is formed on the substrate to isolate the active regions from each other. The gate electrode of the MOS transistors are generally formed by polysilicon, refractory metal or the like. Typically, an oxide insulation layer, containing phosphorus or boron, is applied to the whole surface of the substrate using a CVD (Chemical Vapor Deposition) method. Openings are formed in the oxide insulation layer to expose the diffusion regions of the transistors.

(8) A barrier metal layer then is deposited over the entire oxide insulation layer, and the exposed diffusion regions. The barrier metal layer serves to prevent solid phase epitaxy in the openings of the integrated circuit device employing a conductive pattern, 0.5 micron in width. Materials for the barrier metal layer generally include a refractory material such as MoSi.sub.x (molybdenum silicide), WSi.sub.x (tungsten silicide), or the like, and TiN (titanium nitride). The refractory materials are deposited by a sputtering method, and the TiN is deposited by nitriding titanium or by a reactive sputtering method.

(9) After the barrier metal layer is formed, an aluminum alloy layer is deposited on its entire surface. Known photolithography and etching techniques are applied to the aluminum layer to form fine interconnection layers that extend between the diffusion regions of the different transistors, and to bonding pad regions on the isolation layer. An exterior insulating layer for protecting the integrated circuit from the outside atmosphere and mechanical damage, is then applied. Openings are provided in the protection layer at the bonding pad regions to expose the interconnection layer so that leads may be affixed.

(10) SUMMARY OF THE INVENTION

Details Text Image HTML FULL

US005357136A

United States Patent [19]

Yoshioka

[11] Patent Number: 5,357,136

[45] Date of Patent: Oct. 18, 1994

[54] SEMICONDUCTOR DEVICE WITH ANCHORED INTERCONNECTION LAYER

[75] Inventor: Kentaro Yoshioka, Chiramura, Japan

[73] Assignee: Oki Electric Industry Co., Ltd., Tokyo, Japan

[21] Appl. No.: 42,401

[22] Filed: Apr. 2, 1993

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[52] U.S. Cl. 257/383; 257/384; 257/385; 257/755; 257/751; 257/754; 257/757; 257/764

[58] Field of Search 257/382, 383, 384, 385, 257/739, 751, 755, 757, 764

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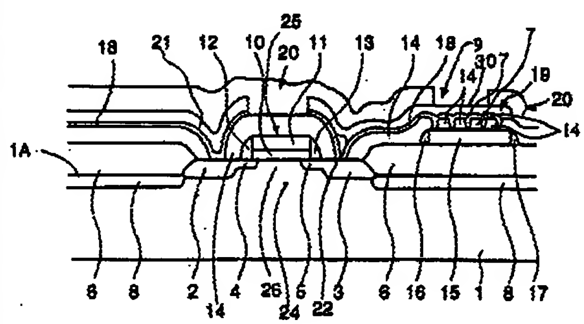
A semiconductor device having a bonding pad region, and a method of its fabrication. A conductive layer is formed on an isolation layer separating transistors of the device, to anchor the interconnection layer on the bonding region. The conductive layer may be formed from the same layer of material that gate electrodes of the transistors are formed. An oxide insulation layer covers the conductive layer and has at least one opening exposing the conductive layer in the bonding pad region. A barrier metal layer, formed on the diffusion regions and the insulation layer, extends into the opening where it makes a firm direct connection with the exposed conductive layer. A bonding pad is formed on the barrier metal layer by providing the interconnection layer on the barrier metal layer. Since the conductive layer and the barrier metal layer are firmly connected, and secures the interconnection layer in the bonding pad structure. According to a method of fabrication, the conductive layer is formed on the isolation layer simultaneously with the formation of the gate electrode, and then covered by the insulation layer. The openings are then provided in the insulation layer to expose the conductive layer. The barrier metal layer is then formed on the insulation layer so that it contacts the diffusion region and extends into the opening to become fixed to the conductive layer. The interconnection layer is thus formed on the conductive layer.

19 Claims, 4 Drawing Sheets



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